The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte GEOFREY S. STRONGIN and DALE E. GULICK

Appeal 2007-1408 Application 09/852,942 Technology Center 2100

Decided: June 18, 2007

Before KENNETH W. HAIRSTON, LEE E. BARRETT, and LANCE LEONARD BARRY, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1 to 29. We have jurisdiction under 35 U.S.C. § 6(b).

Appellants have invented a system and method of selectively coupling a memory to a processor and a bridge. The memory is selectively coupled to the processor and the bridge via a switching mechanism. During a first state,

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the switching mechanism provides access from the processor to the memory, and during a second state, the switching mechanism provides access from the bridge to the memory (Figures 19A to 19C; Specification 60 to 62).

Claim 1 is representative of the claims on appeal, and it reads as follows:

- 1. A system, comprising:
- a processor;
- a bridge coupled to the processor;
- a memory selectably coupled to the bridge and the processor; and

a switching mechanism coupled between the memory and each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Davis	US 5,844,986	Dec. 1, 1998

Chang US 6,286,097 B1 Sep. 4, 2001 (filed Mar. 11, 1999)

The Examiner rejected claims 1 to 4, 10 to 16, 18 to 20, 23 to 26, 28, and 29 under 35 U.S.C. § 102(e) based upon the teachings of Chang. The Examiner rejected claims 5 to 9, 17, 21, 22, and 27 under 35 U.S.C. § 103(a) based upon the teachings of Chang and Davis.

Appellants contend that Chang "does not describe or suggest a switching mechanism that provides a first state providing access from a processor to a memory and a second state providing access from the device to the memory" (Br. 6).

We will sustain all of the rejections of record.

ISSUES

Does the switching mechanism in Chang have a first state that provides access from a processor to a memory, and a second state that provides access from a device to the memory?

FINDINGS OF FACT

Appellants describe a system in which a boot switch 3005 has a first switch position that provides access between a processor 805 and a memory 355, and a second position that provides access between a bridge device 330 and the memory 355 (Figures 19A to 19C; Specification 60-62). All of the claims on appeal provide for the two switching positions.

According to the Examiner's findings, "Chang discloses a computer system for accessing read only memory (ROM) wherein the computer system comprises a main processor (Fig. 8, 310), a bridge coupled to the processor (Fig. 8, 322), a memory selectably coupled to the bridge and the processor (Fig. 8, 350), a switching mechanism coupled between the memory of each of the processor and the bridge, wherein the switching mechanism includes a first state providing access from the processor to the memory and a second state providing access from the bridge to the memory (Fig. 8, 325 & Abstract)" (Answer 3).

In response to Appellants' contention, the Examiner states that "when an individual switching circuit is switched to input B, the claimed limitation of a first state is met because the main processor is connected to the ROM through the B connection in the individual switching circuit [Figure 8 of Chang; col. 7, ll. 44 to 62; Abstract]" (Answer 7). "[W]hen the individual

switching circuit is switched to input A, the claimed limitation of a second state is met because element 322 is connected to the ROM through the A connection in the individual switching circuit" (Answer 7-8).

Davis was cited by the Examiner for a disclosure of "a secure BIOS ROM that is housed within a crypto-processor so that when the computer system boots, the main processor issues a read request for an address corresponding to the BIOS program" (Answer 5).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). The Examiner's articulated reasoning in the rejection must possess a rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

ANALYSIS

We agree with all of the Examiner's findings concerning the teachings of Chang. We additionally agree with the Examiner that all of the limitations of claims 1 to 4, 10 to 16, 18 to 20, 23 to 26, 28, and 29 read directly on the description of Chang.

CONCLUSIONS OF LAW

Anticipation has been established by the Examiner because Chang discloses each and every limitation of the claimed invention set forth in claims 1 to 4, 10 to 16, 18 to 20, 23 to 26, 28, and 29.

Since Appellants have not presented any patentability arguments for claims 5 to 9, 17, 21, 22, and 27 apart from the arguments presented for claim 1, we find that the Examiner has demonstrated the obviousness of these claims.

DECISION

The anticipation rejection of claims 1 to 4, 10 to 16, 18 to 20, 23 to 26, 28, and 29 is affirmed. The obviousness rejection of claims 5 to 9, 17, 21, 22, and 27 is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv).

AFFIRMED

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